

Appl. No. 10/259,889
Amdt. dated December 12, 2003
Reply to Office Action of September 26, 2003

REMARKS/ARGUMENTS

Applicant gratefully acknowledges the thorough Examination to date and has made an effort to fully respond to all the issues raised by the Examiner. Further, the indication of allowable subject matter in Claims 14-18 and 23-24 is greatly appreciated.

In the Specification

In the specification, Applicant amended the specification to add statements of the invention which reflect the language of new independent claims 26, 46, 33 and 47.

In the Drawings

Applicant has provided formal drawings that are believed to comply with the Examiner's objections insofar as such objection can be understood.

Rejection of Claims 1, 10 and 11 under 35 U.S.C. 112

The Examiner has rejected Claims 1-25 as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicant regards as invention. Applicant submits that new Claims 26-42 overcome the Examiner's rejection.

Rejection of Claims 1, 10 and 11 under 35 U.S.C. 102(b)

The Examiner has rejected Claims 1-4 and 6-8 as being anticipated by Vergnes et al. (UPS #5,977,805). The Applicant submits that the new claims 26-42 overcome the Examiner's rejection. However, the Applicant has commented on the cited reference to distinguish the claimed elements of the instant invention from the teachings of the cited reference.

Applicant submits that Vergnes et al. discloses a frequency synthesizer that establishes a desired frequency in a very narrow range centered about a reference frequency of a local oscillator. The frequency synthesizer, taught by Vergnes, includes two-feedback circuits, each of which is connected to a multiplexer. The first feedback circuit generates a plurality of phase signals from a reference frequency generated by an oscillator. The second feedback circuit generates an address signal for the multiplexer,

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which is used to select one of the plurality of phase signals generated by the first feedback circuit as a multiplexer output signal. The multiplexer output is also the frequency synthesizers output. According to Vergnes, by varying the value of an input digital word transmitted to the second feedback circuit, the frequency synthesizer can generate an output frequency which is near the reference frequency that has low jitter and high.

Applicant respectfully submits that the instant invention is novel in view of the Vergnes reference. In his rejection, the Examiner has stated that:

"Vergnes et al. discloses in Figures 1 to 9A-9E a synthesizer circuit comprising a multiphase reference generator (41, 151-153), a multiplier (33, 133), a phase selector (13, 14, 17, 113, 114, 117) having an accumulator (17, 117) responsive to a digital word (11, 111. Note that the output frequency is equal or higher than the reference frequency depending upon the setting of the threshold circuit (14), column 3, lines 40-65."

Applicant respectfully disagrees with the Examiner's statement and submits that the Vergnes synthesizer does not generate an output frequency that is higher than the reference frequency. Applicant submits that Vergnes teaches that an input digital word is transmitted to the shaping circuit 14, which is a modulo accumulator (col 9, lines 18-20). The modulo accumulator generates an overflow signal whenever its value exceeds a predefined threshold. This overflow signal is then transmitted to a second accumulator which generates a digital word that is connected to the address lines of the multiplexer 33. Vergnes teaches that different digital words are used to select the various phase delayed signals as the multiplexer output 35 in order to compensate for jitter in the reference frequency. By selecting the phase delay signals in the sequence described by Vergnes (col. 4, lines 39), the frequency synthesizer can generate an output frequency near the reference frequency with low jitter.

In contrast to Vergnes, Applicant submits that the instant invention synthesizes a frequency that is higher than an input frequency based on an input signal and a predetermined control word. Applicant submits that unlike the Vergnes synthesizer, the instant invention includes only a single feedback circuit which selects successive phase delayed signals in order to produce a higher output frequency. Applicant further submits that the instant invention is more elegant and simpler than the frequency

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synthesizer disclosed by Vergnes. In the frequency synthesizer of the instant, the output of the multiplexer is connected directly to its select ports as oppose to a shaping circuit. Furthermore, the predetermined control signal is connected directly to the phase selector as oppose to a shaping circuit as in Vergnes. The instant invention is easier to manufacture than the one taught by Vergnes and that it is less expensive to produce. Therefore, in view of the differences between the claimed invention and the cited reference, Applicant respectfully submits that new claims are novel in view of the Vergnes et al. reference.

Rejection of Claims 1, 10 and 11 under 35 U.S.C. 103(a)

The Examiner has rejected Claims 1-4 and 6-8 as being obvious in view of Vergnes et al. (UPS #5,977,805). Applicant submits that new claims 26-42 overcome the Examiner's rejection. Furthermore, Applicant submits that the comments made above are equally applicable in regard to the Examiner's rejection, and therefore submits that the subject matter of new claims 26-42 are not obvious in view of the Vergnes et al. reference.

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Conclusion

Applicant respectfully submits that the rejections under 35 USC 112, 35 USC 102 and 35 USC 103 have been overcome by the above amendments and remarks. Applicant respectfully submits that all of the claims presently standing in the application are patentably distinguished from teachings of the Vergnes et al. patent. Accordingly, reconsideration and allowance of this application is respectfully solicited.

The Commissioner is hereby authorized to debit any underpayment or credit any overpayment to the USPTO deposit account no. 16-0600 should any additional fees be necessary.

Respectfully Submitted,
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